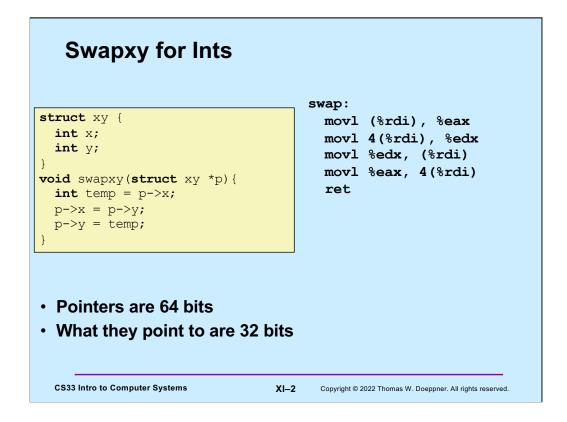
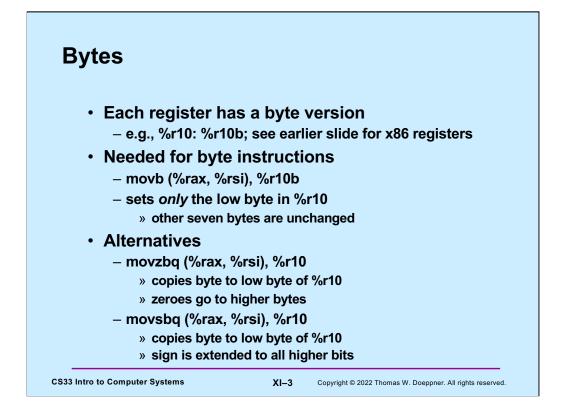


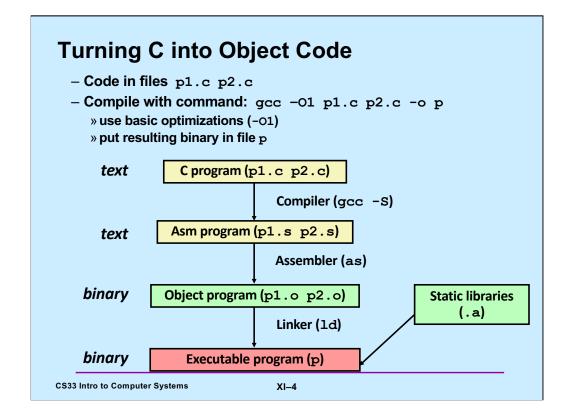
Most of the slides in this lecture are either from or adapted from slides provided by the authors of the textbook "Computer Systems: A Programmer's Perspective," 2nd Edition and are provided from the website of Carnegie-Mellon University, course 15-213, taught by Randy Bryant and David O'Hallaron in Fall 2010. These slides are indicated "Supplied by CMU" in the notes section of the slides.



Here we have a simple function that swaps the two components of a structure that's passed to it. (Assume that %rdi contains the argument.) Note that even though we use the "e" form of the registers to hold the (32-bit) data, we need the "r" form to hold the 64-bit addresses.



Note that using single-byte versions of registers has a different behavior from using 4byte versions of registers. Putting data into the latter using **mov** causes the upper bytes to be zeroed. But with the byte versions, putting data into them does not affect the upper bytes.



Note that normally one does not ask gcc to produce assembler code, but instead it compiles C code directly into machine code (producing an object file). Note also that the gcc command actually invokes a script; the compiler (also known as gcc) compiles code into either assembler code or machine code; if necessary, the assembler (as) assembles assembler code into object code. The linker (ld) links together multiple object files (containing object code) into an executable program.

Example

```
long ASum(long *a, unsigned long size) {
    long i, sum = 0;
    for (i=0; i<size; i++)
        sum += a[i];
    return sum;
  }
int main() {
    long array[3] = {2,117,-6};
    long sum = ASum(array, 3);
    return sum;
  }
CS33 Intro to Computer Systems
  XI-5 Copyright & 2022 Theorem 2.1 in the form of the system 2.2
</pre>
```

		bler Code			
Sum:			main:		
	testq	%rsi, %rsi		subq	\$32, %rsp
	je	.L4		movq	
	movq	%rdi, %rax		movq	
	leaq	(%rdi,%rsi,8), %rcx		movq	· · · · · · · · · · · · · · · · · · ·
	movl	\$0, %edx		movq	1 ·
L3:				movl	\$3, %esi
	addq	(%rax), %rdx		call	ASum
	addq	\$8, %rax		addq	\$32, %rsp
	cmpq	%rcx, %rax		ret	
	jne	.L3			
L1:					
	movq	%rdx, %rax			
	ret				
L4:					
	movl	\$0, %edx			
	jmp	.L1			

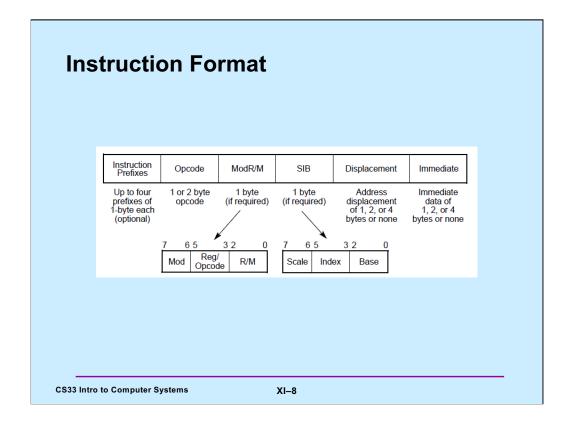
Here is the assembler code produced by gcc from the C code of the previous slide. Note that the two movl instructions are ostensibly just copying a zero into %edx (a 32-bit register). However, what it's really doing is copying a zero in the 64-bit register %rdx (the 64-bit extension of %edx). This happens because, as we discussed earlier, when one copies something into a 32-bit register, the high-order 32 bits of its extension is filled with 0s.

Code for ASum		
0x1125 <asum>: 0x48 0x85</asum>	•	Assembler – translates .s into .o – binary encoding of each instruction
0xf6 0x74 0x1c		 nearly complete image of executable code missing linkages between code in
0x48 0x89 0xf8	•	different files
	of 39 bytes instruction: or 3 bytes	 resolves references between files combines with static run-time libraries
• Starts 0x11	at address 25	 » e.g., code for printf – some libraries are dynamically linked » linking occurs when program begins execution

Adapted from a slide supplied by CMU.

The lefthand column shows the object code produced by gcc. This was produced either by assembling the code of the previous slide, or by compiling the C code of the slide before that.

Suppose that all we have is the object code – we don't have the assembler code and the C code. Can we translate for object code to assembler code? (This is known as disassembling.)



This is taken from Intel 64 and IA-32 Architecture Software Developer's Manual, Volume 2: Instruction Set Reference; Order Number 325462-043US, Intel Corporation, May 2012 (<u>https://software.intel.com/en-us/download/intel-64-and-ia-32-architectures-sdm-combined-volumes-1-2a-2b-2c-2d-3a-3b-3c-3d-and-4</u>)

The point of the slide is that the instruction format is complicated, too much so for a human to deal with. Which is why we talk about **disassemblers** in the next slides.

25 <asum>: 48 85 f6</asum>		
48 85 f6		
	test	%rsi,%rsi
74 1c	je	1146 <asum+0x21></asum+0x21>
48 89 £8	mov	<pre>%rdi,%rax</pre>
48 8d 0c f7	lea	(%rdi,%rsi,8),%r
ba 00 00 00 00		1 /
48 03 10	add	(%rax),%rdx
48 83 c0 08	add	\$0x8,%rax
48 39 c8	cmp	<pre>%rcx,%rax</pre>
75 f4	jne	1136 <asum+0x11></asum+0x11>
48 89 d0	mov	<pre>%rdx,%rax</pre>
c3	retq	
	mov	\$0x0,%edx
eb f5	jmp	1142 < ASum + 0x1d >
er <file></file>		
	48 8d 0c f7 ba 00 00 00 00 48 03 10 48 83 c0 08 48 39 c8 75 f4 48 89 d0 c3 ba 00 00 00 00 eb f5	48 8d 0c f7 lea ba 00 00 00 mov 48 03 10 add 48 03 10 add 48 83 c0 08 add 48 83 c0 08 add 48 39 c8 cmp 75 75 f4 jne 48 89 d0 mov c3 retq ba 00 00 00 mov eb f5 jmp jmp

Adapted from a slide supplied by CMU.

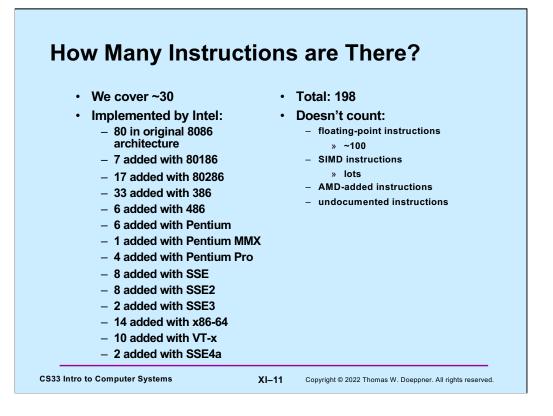
objdump's rendition is approximate because it assumes everything in the file is assembly code, and thus translates data into (often really weird) assembly code. Also, it leaves off the suffix at the end of each instruction, assuming it can be determined from context.

Object	Disassembled
0x1125:	Dump of assembler code for function ASum:
0x48 0x85	0x1125 <+0>: test %rsi,%rsi
0x85 0xf6	0x1128 <+3>: je 0x1146 <asum+33></asum+33>
0x10	0x112a <+5>: mov %rdi,%rax
0x1c	0x112d <+8>: lea (%rdi,%rsi,8),%rc
0x48	0x1131 <+12>: mov \$0x0,%edx
0x89	
0xf8	
0x48	. Within adh dehuarar
0x8d	 Within gdb debugger
0x0c	gdb <file></file>
0xf7	disassemble ASum
•	 disassemble the ASum object code
•	· · · · · · · · · · · · · · · · · · ·
•	x/39xb ASum

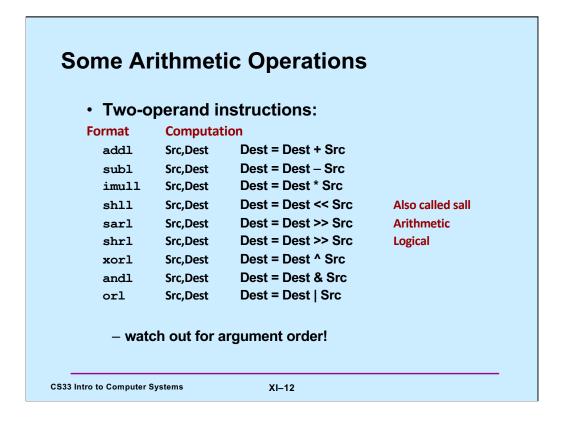
Adapted from a slide supplied by CMU.

The x/35xb'' directive to gdb says to examine (first x, meaning print) 35 bytes (b) viewed as hexadecimal (second x) starting at ASum.

The format of the output has been modified a bit from what gdb actually produces, so that it will fit on the slide. In the dump of the assembler code, the addresses are actually 64-bit values (in hex) – we have removed the leading 0s. The output of the x command is actually displayed in multiple columns. We have reorganized it into one column.



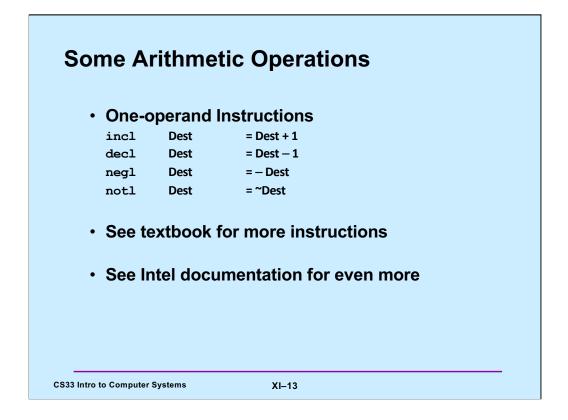
The source for this is http://en.wikipedia.org/wiki/X86_instruction_listings, viewed on 6/20/2017, which came with the caveat that it may be out of date. While it's likely that more instructions have been added since then, we won't be covering them in 33!



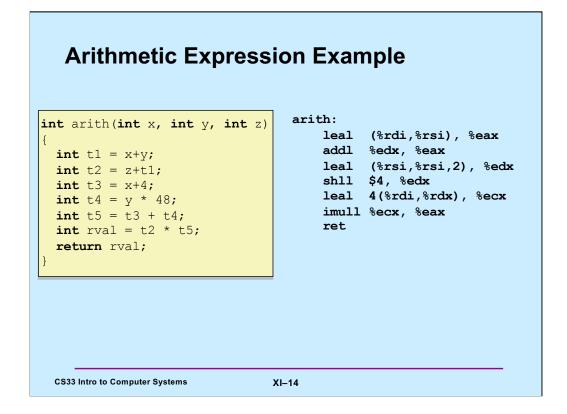
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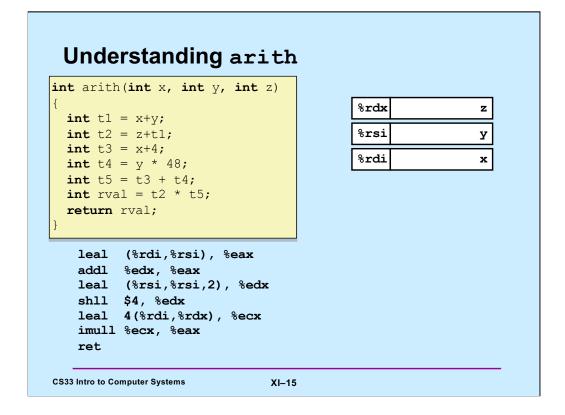
Note that for shift instructions, the Src operand (which is the size of the shift) must either be an immediate operand or be a designator for a one-byte register (e.g., %cl – see the slide on general-purpose registers for IA32).

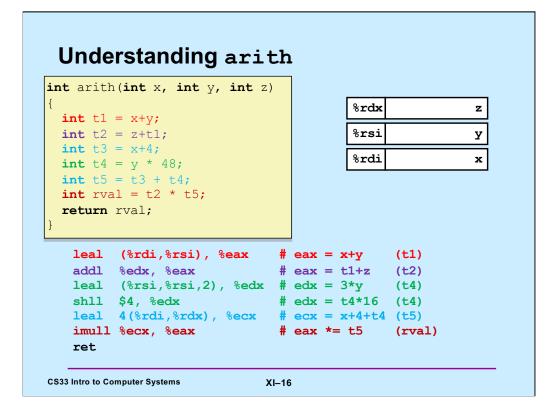
Also note that what's given in the slide are the versions for 32-bit operands. There are also versions for 8-, 16-, and 64-bit operands, with the "l" replaced with the appropriate letter ("b", "s", or "q").



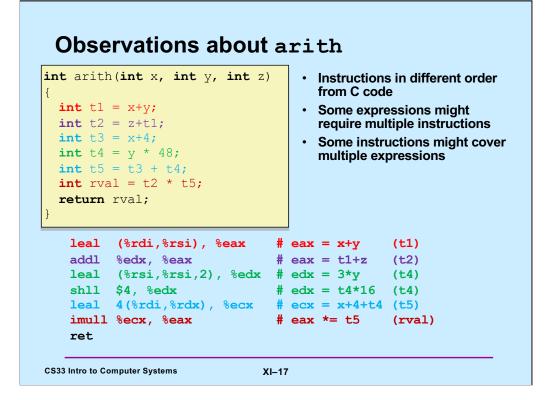
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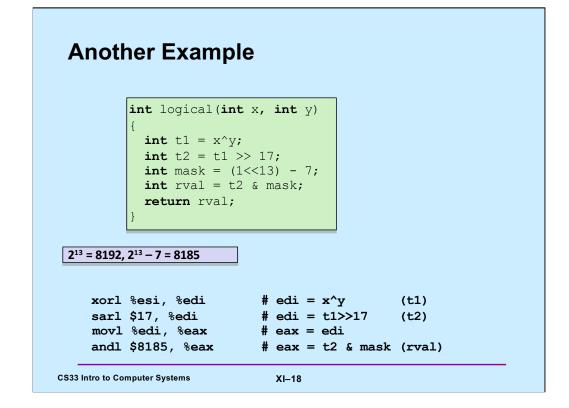


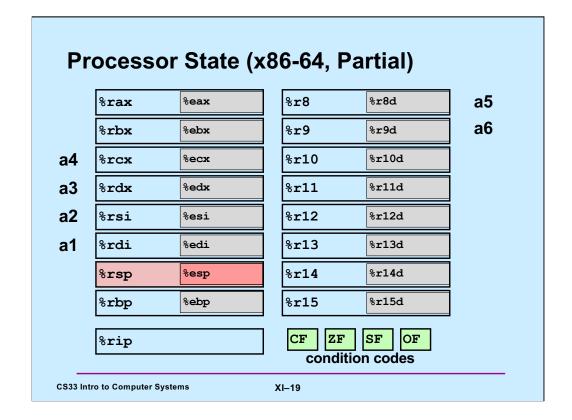




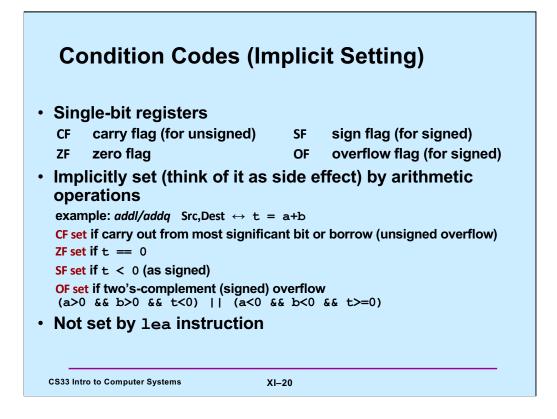
By convention, the first three arguments to a function are placed in registers **rdi**, **rsi**, and **rdx**, respectively. Note that, also by convention, functions put their return values in register **eax/rax**.

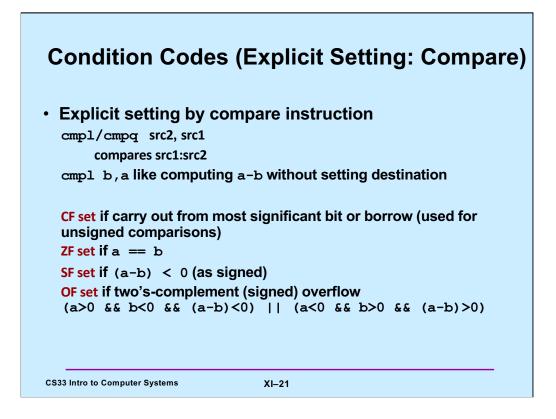






%rip is the instruction-pointer register. It contains the address of the next instruction to be executed. CF, ZF, SF, and OF are the condition codes, referring to carry flag, zero flag, sign flag, and overflow flag.





Condition Codes (Explicit Setting: Test)	
 Explicit setting by test instruction 	
test1/testq src2, src1 test1 b,a like computing a&b without setting destination	
– sets condition codes based on value of Src1 & Src2	
 useful to have one of the operands be a mask 	
ZF set when a&b == 0	
SF set when a &b < 0	
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Note that if a&b<0, what is meant is that the most-significant bit is 1.

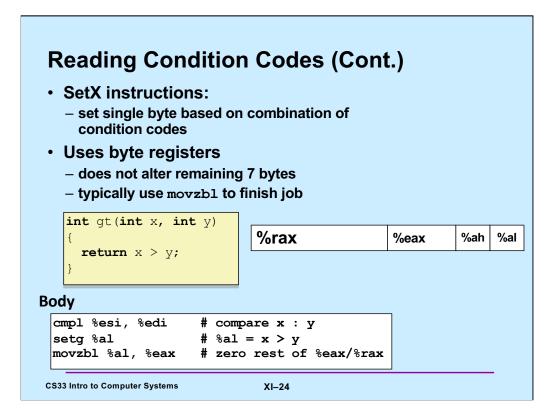
ading	Condition	Codes
etX inst	ructions	
set sinal	e byte based on co	ombinations of condition cod
	-	
SetX	Condition	Description
sete	ZF	Equal / Zero
setne	~ZF	Not Equal / Not Zero
sets	SF	Negative
setns	~SF	Nonnegative
setg	~(SF^OF) &~ZF	Greater (Signed)
setge	~ (SF^OF)	Greater or Equal (Signed)
setl	(SF^OF)	Less (Signed)
setle	(SF^OF) ZF	Less or Equal (Signed)
seta	~CF&~ZF	Above (unsigned)
setb	CF	Below (unsigned)
L		

These operations allow one to set a byte depending on the values of the condition codes.

Some of these conditions aren't all that obvious. Suppose we are comparing A with B (cmpl B,A). Thus the condition codes would be set as if we computed A-B. For signed arithmetic, If A >= B, then the true result is non-negative. But some issues come up because of two's complement arithmetic with a finite word size. If overflow does not occur, then the sign flag should not be set. If overflow does occur (because A is positive, B is negative, and A-B is a large positive number that does not fit in an int), then even though the true result should have been positive, the actual result is negative. So, if both the sign flag and the overflow flag are not set, we know that A >= B. If both flags are set, we know the true result of the subtraction is positive and thus A>=B. But if one of the two flags is set and the other isn't, then A must be less than B. Thus if ~(SF^OF) is 1, we know that A>=B. If ZF (zero flag) is set, we know that A==B. Thus for A>B, ZF is not set.

For unsigned arithmetic, if A>B, then subtracting B from A doesn't require a borrow and thus CF is not set; and since A is not equal to B, ZF is not set. If A<B, then subtracting B from A requires a borrow and thus CF is set.

The other cases can be worked out similarly.



Recall that the first argument to a function is passed in %rdi (%edi) and the second in %rsi (%esi).

Jumping

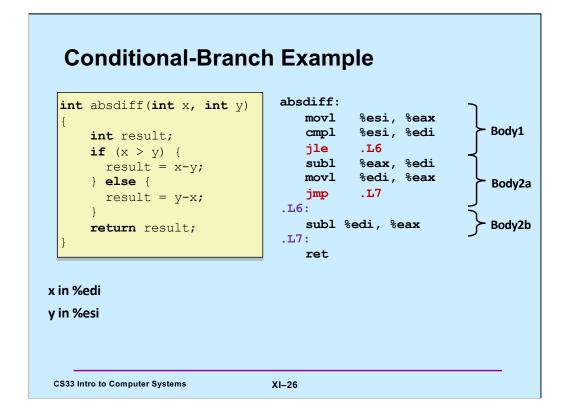
• jX instructions

– Jump to different part of program depending on condition codes

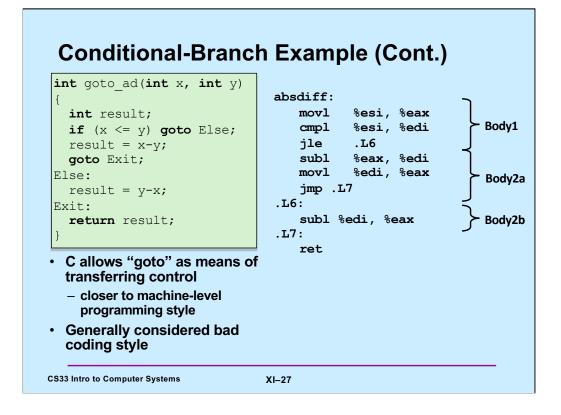
jХ	Condition	Description
jmp	1	Unconditional
je	ZF	Equal / Zero
jne	~ZF	Not Equal / Not Zero
js	SF	Negative
jns	~SF	Nonnegative
jg	~ (SF^OF) &~ZF	Greater (Signed)
jge	~ (SF^OF)	Greater or Equal (Signed)
jl	(SF^OF)	Less (Signed)
jle	(SF^OF) ZF	Less or Equal (Signed)
ja	~CF&~ZF	Above (unsigned)
jb	CF	Below (unsigned)

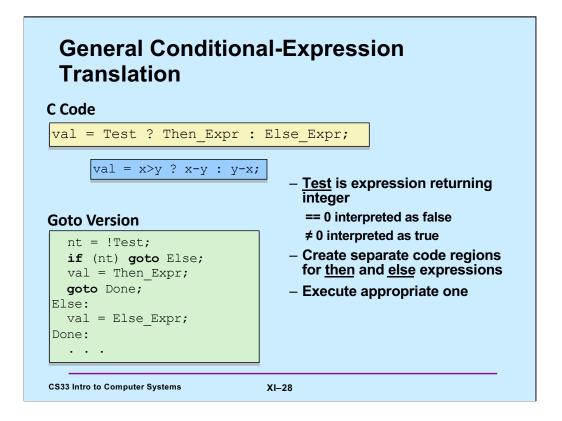
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See the notes for slide 23.

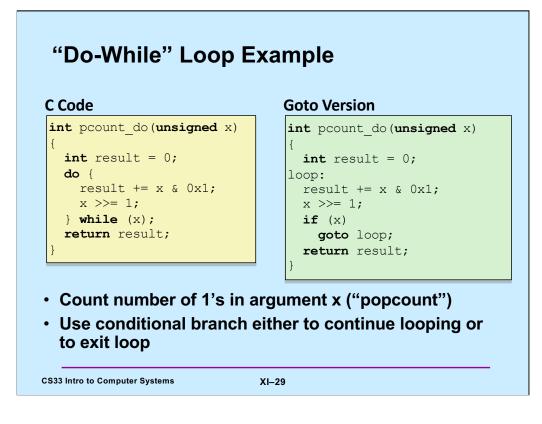


The function computes the absolute value of the difference of its two arguments.



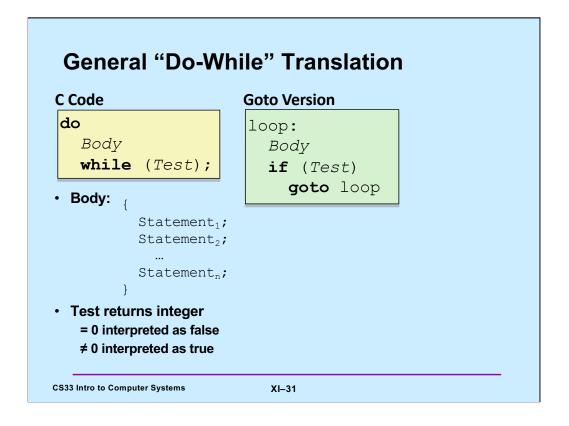


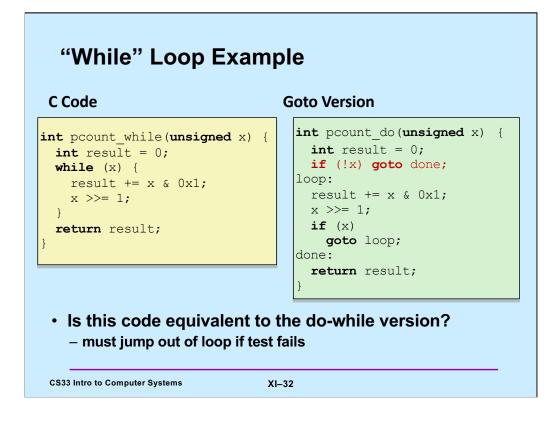
C's conditional expression, as shown in the slide, is sometimes useful, but often results in really difficult-to-read code.

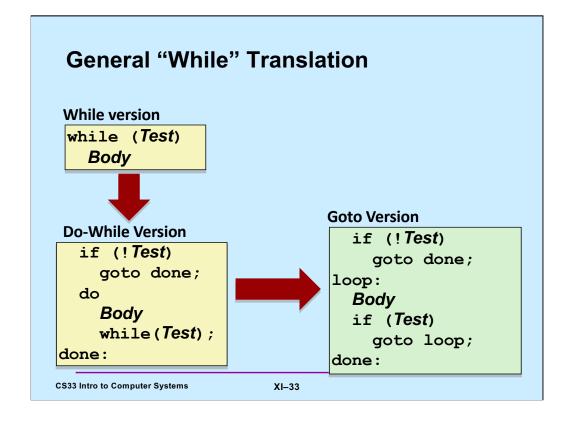


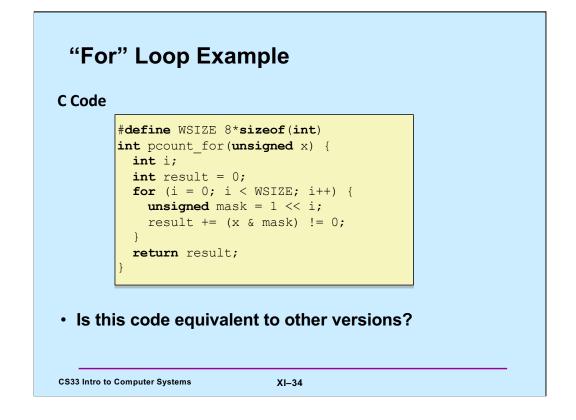
"Do-While	" Loor	Compile	atio	n
Goto Version		oompin		
<pre>int pcount_do(uns int result = 0; loop: result += x & 0 x >>= 1;</pre>	-	{		
<pre>if (x) goto loop; return result; }</pre>				
	.12:	\$0, %eax # loop: %edi, %ecx	#	result = 0
Registers: %edi x %eax result	addl shrl	\$1, %ecx %ecx, %eax %edi	# #	t = x & 1 result += t x >>= 1 if 10 gets leep
CS33 Intro to Computer Syste	jne	%edi .L2 XI-30	# #	

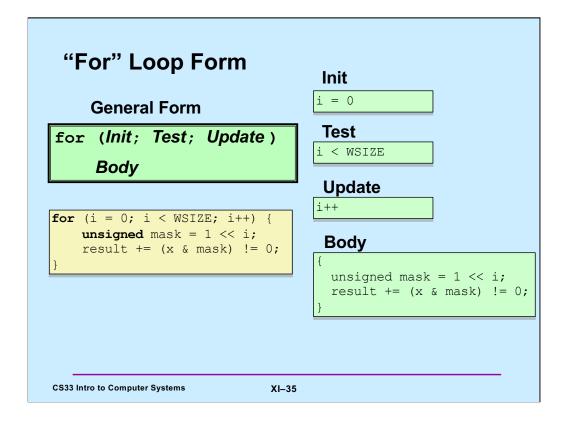
Note that the condition codes are set as part of the execution of the **shrl** instruction.



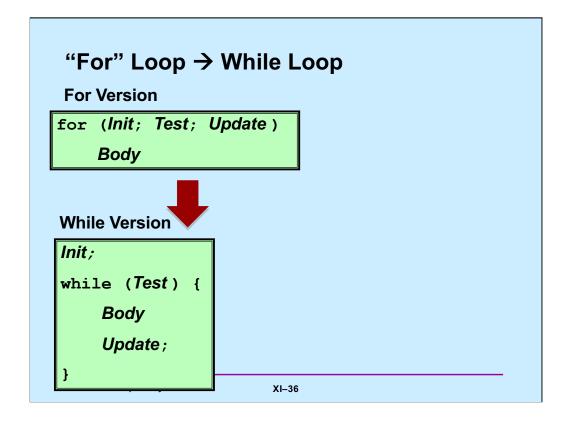


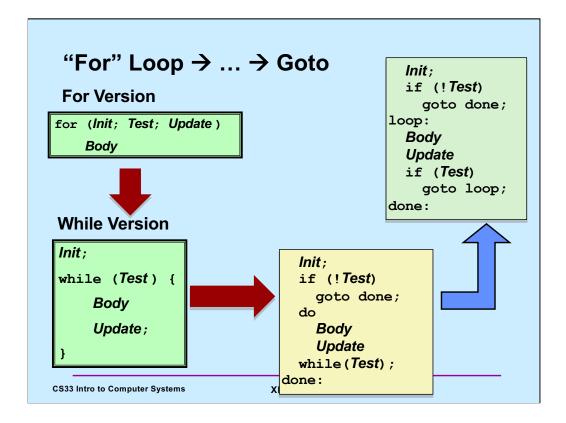




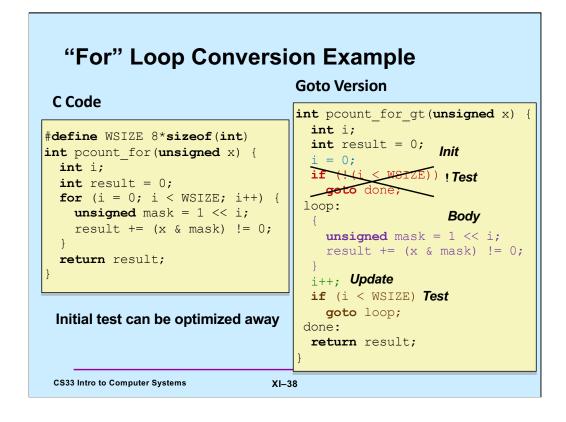


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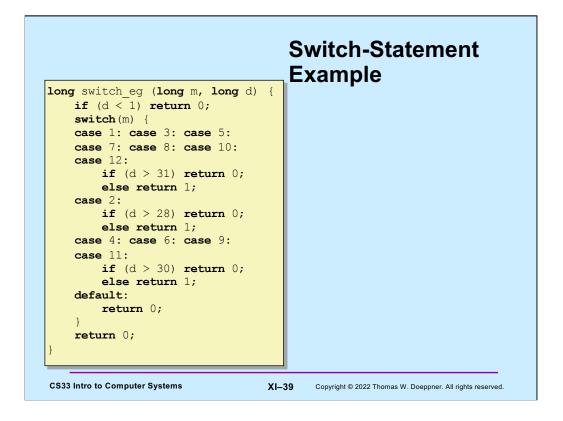




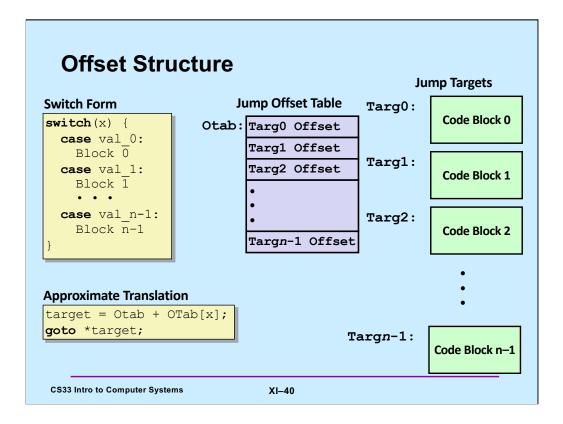
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Code very much like this appears in level three of the traps project.



Adapted from slide supplied by CMU to account for changes in gcc.

The translation is "approximate" because C doesn't have the notion of the target of a goto being a variable. But, if it did, then the translation is what we'd want!

Otab (for "offset table") is a table of relative address of the jump targets. The idea is, given a value of x, **Otab**[x] contains a reference to the code block that should be handled for that case in the switch statement (this code block is known as the **jump target**). These references are offsets from the address **Otab**. In other words, **Otab** is an address, if we add to it the offset of a particular jump target, we get the absolute address of that jump target.

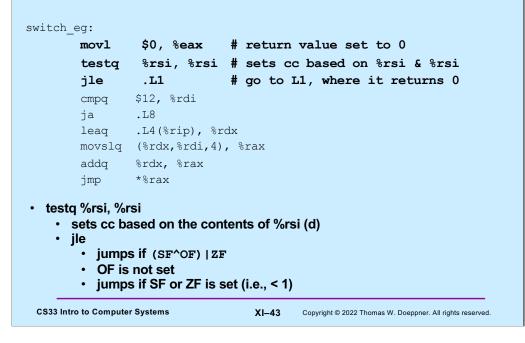
<pre>switch_eg: .section .rodata movl \$0, %eax .align 4 testq %rsi, %rsi .L4: jle .L1 .long .L8L4 ja .L8 leaq .L4(%rip), %rdx .long .L3L4 movslq (%rdx, %rdi, 4), %rax .long .L5L4 addq %rdx, %rax .long .L5L4 jmp *%rax .long .L5L4 .long .L3L4 .long .L3L4</pre>	Assemb	oler Code (1)			
.long .L3L4	movl testq jle cmpq ja leaq movslq addq	<pre>%rsi, %rsi .L1 \$12, %rdi .L8 .L4(%rip), %rdx (%rdx,%rdi,4), %rax %rdx, %rax</pre>	.L4:	.align 4 .long .long .long .long .long .long .long .long .long .long .long .long	.L8L4 .L3L4 .L5L4 .L5L4 .L5L4 .L5L4 .L5L4 .L3L4 .L3L4 .L5L4 .L5L4 .L5L4 .L5L4

Here's the assembler code obtained by compiling our C code in gcc with the -O1 optimization flag (specifying that some, but not lots of optimization should be done). We explain this code in subsequent slides. The jump offset table starts at label .L4.

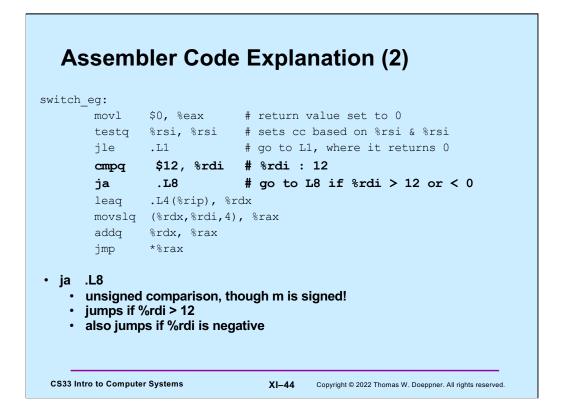
Assembler Code (2)

.L3:			.L5:		
	cmpq	\$31, %rsi		cmpq	\$30, %rsi
	setle	%al		setle	%al
	movzbl	%al, %eax		movzbl	%al, %eax
	ret			ret	
.L6:			.L8:		
	cmpq	\$28, %rsi		movl	\$0, %eax
	setle	%al	.L1:		
	movzbl	%al, %eax		ret	
	ret				
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Assembler Code Explanation (1)



The first three instructions cause control to go to .L1 if the second argument (d) is less than 1. At .L1 is code that simply returns (with a return value of 0).



The next two instructions simply check to make sure that %rsi (the first argument, m) is less than or equal to 12. If not, control goes to .L8, which sets the return value to 0 and returns. Of course, the return value (in $\frac{\pi x}{\theta}$ is already zero, so setting it to zero again is unnecessary.

Note that we're using **ja** (jump if above), which is normally used after comparing unsigned values. The first argument, m, is a (signed) **long**. But if it is interpreted as an unsigned value, then if the leftmost bit (the sign bit) is set, it appears to be a very large unsigned value, and thus the jump is taken.

Assembler Code Expla	nation (3)
switch_eg: movl \$0, %eax testg %rsi, %rsi	.section .rodata .align 4 .L4:
<pre>jle .L1 cmpq \$12, %rdi ja .L8 leaq .L4(%rip), %rdx movslq (%rdx,%rdi,4), %rax addq %rdx, %rax jmp *%rax</pre>	<pre>.long .L8L4 # m=0 .long .L3L4 # m=1 .long .L6L4 # m=2 .long .L3L4 # m=3 .long .L5L4 # m=4 .long .L3L4 # m=5 .long .L3L4 # m=6 .long .L3L4 # m=7 .long .L3L4 # m=8 .long .L3L4 # m=9 .long .L3L4 # m=10 .long .L3L4 # m=11 .long .L3L4 # m=12</pre>
CS33 Intro to Computer Systems XI–45	Copyright © 2022 Thomas W. Doeppner. All rights reserved.

The table on the right is known as an **offset table**. Each line refers to the code to be executed for the corresponding value of m. Each entry in the table is a long (recall that in x86-64 assembler, long means 32 bits). The value of each entry is the difference between the address of the table (.L4) and the address of the code to be executed for a particular value of m (the other .L labels). Thus each entry is the distance (or offset) from the beginning of the table to the code for each case. Note that this offset might be negative. It's assumed that the offset fits in a 32-bit signed quantity (which the system guarantees to be true.)

One might ask why we put 32-bit offsets in the table rather than 64-bit addresses. The reason is to reduce the size of these tables – if we used addresses, they'd be twice the size.

This table is not executable (it just contains offsets), but it also should be treated as read-only – its contents will never change. The directive ".section .rodata" tells the assembler that we want this table to be located in memory that is read-only, but not executable. The directive at the end of the table (".text")tells the assembler that what follows is (again) executable code.

The highlighted code on the left is what interprets the table, We examine it next.

<pre>switch_eg: mov1 \$0, %eax testq %rsi, %rsi jle .L1 cmpq \$12, %rdi ja .L8 leaq .L4(%rip), %rdx movslq (%rdx,%rdi,4), %rax addq %rdx, %rax jmp *%rax indirect jump long .L3L4 # m=3 long .L3L4 # m=4 long .L3L4 # m=4 long .L3L4 # m=5 long .L3L4 # m=5 long .L3L4 # m=7 long .L3L4 # m=7 long .L3L4 # m=8 long .L3L4 # m=10 long .L3L4 # m=10 long .L3L4 # m=12 </pre>	Assembler Code Expla	nation (4)
ja .L8 .long .L6L4 # m=2 leaq .L4(%rip), %rdx .long .L3L4 # m=3 movslq (%rdx,%rdi,4), %rax .long .L5L4 # m=4 addq %rdx, %rax .long .L5L4 # m=5 .long .L5L4 # m=5 .long .L5L4 # m=6 .long .L3L4 # m=7 .long .L3L4 # m=7 .long .L3L4 # m=8 .long .L3L4 # m=8 .long .L3L4 # m=10 .long .L3L4 # m=10	movl \$0, %eax testq %rsi, %rsi jle .Ll	.align 4 .L4: .long .L8L4 # m=0
.long .L3L4 # m=10 .long .L5L4 # m=11	<pre>ja .L8 leaq .L4(%rip), %rdx movslq (%rdx,%rdi,4), %rax addq %rdx, %rax jmp *%rax indirect</pre>	.long .L6L4 # m=2 .long .L3L4 # m=3 .long .L5L4 # m=4 .long .L3L4 # m=5 .long .L5L4 # m=6 .long .L3L4 # m=7 .long .L3L4 # m=8
CS33 Intro to Computer Systems XI-46 Copyright © 2022 Thomas W. Doeppner. All rights reserved.		.long .L3L4 # m=10 .long .L5L4 # m=11 .long .L3L4 # m=12 .text

The highlighted code makes use of an indirect jump instruction, indicated by having an asterisk before its register operand. The register contains an address, and the jump is made to the code at that address.

Assembler Code Explanation	n (5)
switch_eg: movl \$0, %eax testq %rsi, %rsi . L4 :	.section .rodata .align 4
<pre>jle .L1 cmpq \$12, %rdi ja .L8 leaq .L4(%rip), %rdx movslq (%rdx,%rdi,4), %rax addq %rdx, %rax jmp *%rax</pre>	.long .L8L4 # m=0 .long .L3L4 # m=1 .long .L6L4 # m=2 .long .L3L4 # m=3 .long .L5L4 # m=4 .long .L3L4 # m=5 .long .L5L4 # m=6 .long .L3L4 # m=7 .long .L3L4 # m=8 .long .L5L4 # m=9 .long .L5L4 # m=10 .long .L5L4 # m=11 .long .L3L4 # m=12 .text
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The **leaq** instruction (load effective address, quad), performs an address computation, but rather than fetching the data at the address, it stores the address itself in %rdx.

What's unusual about the instruction is that it uses %rip (the instruction pointer) as the base register, and has a displacement that is a label. This is a special case for the assembler, which can compute the offset between the leaq instruction and the label, and use that value for the displacement field.

Assembler Code Explanation	on (6)
<pre>switch_eg: mov1 \$0, %eax testq %rsi, %rsi .L4: jle .L1 cmpq \$12, %rdi ja .L8 leaq .L4(%rip), %rdx movslq (%rdx,%rdi,4), %rax addq %rdx, %rax jmp *%rax</pre>	.section .rodata .align 4 .long .L8L4 # m=0 .long .L3L4 # m=1 .long .L6L4 # m=2 .long .L3L4 # m=3 .long .L5L4 # m=4 .long .L3L4 # m=5 .long .L5L4 # m=6 .long .L3L4 # m=7
CS22 Inter to Computer Suptema	.long .L3L4 # m=8 .long .L5L4 # m=9 .long .L3L4 # m=10 .long .L5L4 # m=11 .long .L5L4 # m=12 .text
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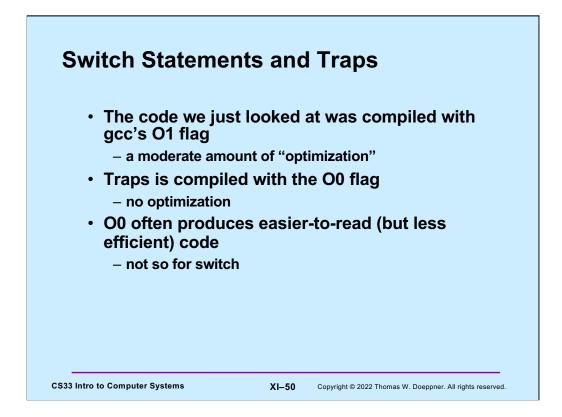
The **movslq** instruction copies a long (32 bits) into a quad (64 bits), and does sign extension so as to preserve the sign of the value being copied.

%rdi contains m, the first argument, which is also the argument of the switch statement. We use it to index into the offset table: As we saw in the previous slide, %rdx contains the address of the table, whose entries are each 4 bytes long. Thus we use %rdi as an index register, with a scale factor of 4. The contents of that entry (which is the distance from the table to the code that should be executed to handle this case) is copied into %rax, using sign extension to fill the register.

Assembler Code Explanation	on (7)
switch_eg: movl \$0, %eax testg %rsi, %rsi .L4:	.section .rodata .align 4
<pre>jle .L1 cmpq \$12, %rdi ja .L8 leaq .L4(%rip), %rdx movslq (%rdx,%rdi,4), %rax addq %rdx, %rax jmp *%rax</pre>	.long .L8L4 # m=0 .long .L3L4 # m=1 .long .L6L4 # m=2 .long .L3L4 # m=3 .long .L5L4 # m=4 .long .L3L4 # m=5 .long .L3L4 # m=6 .long .L3L4 # m=7 .long .L3L4 # m=8 .long .L3L4 # m=9 .long .L3L4 # m=10 .long .L3L4 # m=11 .long .L3L4 # m=12 .text
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The offset of the code we want to jump to is in %rax. To convert this offset into an absolute address, we need to add to it the address of the table. That's what the **addq** instruction does.

We can now do the indirect jump, to the address contained in %rax.



itch_eg01		switch_eg0	
	\$0, %eax	pushq	*
testq	%rsi, %rsi	movq	%rsp, %rbp
jle		-	%rdi, -8(%rbp)
cmpq	\$12, %rdi	movq	%rsi, -16(%rbp)
ja	.L8	cmpq	\$0, -16(%rbp)
leaq	.L4(%rip), %rdx	jg	.L2
movslq	(%rdx,%rdi,4), %rax	movl	\$0, %eax
addq	%rdx, %rax	jmp	.L3
jmp	*%rax	.L2:	
		cmpq	\$12, -8(%rbp)
		ja	.L4
		movq	-8(%rbp), %rax
		leaq	0(,%rax,4), %rdx
		leaq	.L6(%rip), %rax
		movl	(%rdx,%rax), %eax
		cltq	
		leag	.L6(%rip), %rdx
		-	%rdx, %rax
		jmp	

On the left we have the O1 version of the code, on the right we have the O0.

itch eq01	:	switch eg0():
	\$0, %eax	pushq	
testq	%rsi, %rsi	movq	<pre>%rsp, %rbp</pre>
jle	.L1		<pre>%rdi, -8(%rbp)</pre>
cmpq	\$12, %rdi	movq	%rsi, -16(%rbp)
ja	.18	cmpq	\$0, -16(%rbp)
leaq	.L4(%rip), %rdx	jg	.L2
movslq	(%rdx,%rdi,4), %rax	movl	\$0, %eax
addq	%rdx, %rax	jmp	.L3
jmp	*%rax	.L2:	
		cmpq	\$12, -8(%rbp)
		ja	.L4
		movq	-8(%rbp), %rax
		leaq	0(,%rax,4), %rdx
		leaq	.L6(%rip), %rax
		movl	(%rdx,%rax), %eax
		cltq	
		leaq	.L6(%rip), %rdx
		addq	%rdx, %rax
		jmp	*%rax

The highlighted code is not present in the O1 version. It links this function's stack frame to its caller, something we'll talk about in the next lecture. It also (rather inexplicably) copies the arguments from the registers to the stack frame.

			_
itch_eg01		switch_eg0(
	\$0, %eax	pushq	*
-	%rsi, %rsi		%rsp, %rbp
jle			%rdi, -8(%rbp)
	\$12, %rdi	-	%rsi, -16(%rbp)
ja	.18	cmpq	\$0, -16(%rbp)
leaq	.L4(%rip), %rdx	ja	.12
movslq	(%rdx,%rdi,4), %rax	movl	\$0, %eax
addq	%rdx, %rax	jmp	.13
jmp	*%rax	.L2:	
		cmpq	\$12, -8(%rbp)
		ja	.L4
		movq	-8(%rbp), %rax
		leaq	0(,%rax,4), %rdx
		leaq	.L6(%rip), %rax
		movl	(%rdx,%rax), %eax
		cltq	
		leag	.L6(%rip), %rdx
		-	%rdx, %rax
		jmp	*%rax

The next four instructions compare the second argument (d) with 0; if it's less than or equal to zero, it returns 0 (.L3 is the label of code that simply returns). Otherwise it jumps to .L2.

:+-h01		it-h0	
itch_eg01	\$0, %eax	switch_eg0(pushq	
	%rsi, %rsi		%rsp, %rbp
ile			%rdi, -8(%rbp)
2	\$12, %rdi		%rsi, -16(%rbp)
ja		-	\$0, -16(%rbp)
-	.L4(%rip), %rdx	ia	
-	(%rdx,%rdi,4), %rax		\$0, %eax
addq	%rdx, %rax	jmp	.L3
jmp	*%rax	.L2:	
		cmpq	\$12, -8(%rbp)
		ja	. 1.4
		movq	-8(%rbp), %rax
		leaq	0(,%rax,4), %rdx
		leaq	.L6(%rip), %rax
		movl	(%rdx,%rax), %eax
		cltq	
		leaq	.L6(%rip), %rdx
		addq	%rdx, %rax
		jmp	*%rax

The next two instructions do the same thing as the **cmpq** and **ja** instructions do in the O1 code. If the first argument (m) is greater than 12 or less than 0, these instructions cause a jump (in this case to .L4, which labels what's essentially the same code as is labelled by .L8 in the O1 code) to code that returns 0.

itch eq01		switch eq00	· ·
	\$0, %eax	pushq	
	%rsi, %rsi		%rsp, %rbp
ile			%rdi, -8(%rbp)
2	\$12, %rdi		%rsi, -16(%rbp)
ja	.L8	cmpq	\$0, -16(%rbp)
leaq	.L4(%rip), %rdx	jg	.L2
movslq	(%rdx,%rdi,4), %rax	movl	\$0, %eax
addq	%rdx, %rax	jmp	.L3
jmp	*%rax	.L2:	
		cmpq	\$12, -8(%rbp)
		ja	.L4
		movq	-8(%rbp), %rax
		leaq	0(,%rax,4), %rdx
		leaq	.L6(%rip), %rax
		movl	(%rdx,%rax), %eax
		cltq	
		leaq	.L6(%rip), %rdx
		addq	%rdx, %rax
		jmp	*%rax

In the next three instructions, the first one copies the first argument (m, which had been earlier copied to the stack) to %rax. Recall that m is the argument to the switch statement, and will be used as an index into the jump table.

The first **leaq** statement computes four times %rax, and puts the result into %rdx. The next **leaq** statement does the same thing as the **leaq** statement of the O1 code, it computes the address of the offset table (which is labelled with .L6 in this version) and stores it in %rax.

	-	planation	(-)
itch_eg01	:	switch_eg00	0:
movl	\$0, %eax	pushq	%rbp
testq	%rsi, %rsi	movq	%rsp, %rbp
jle	.L1	movq	%rdi, -8(%rbp)
cmpq	\$12, %rdi	movq	%rsi, -16(%rbp)
ja	.L8	cmpq	\$0, -16(%rbp)
leaq	.L4(%rip), %rdx	jg	.L2
movslq	(%rdx,%rdi,4), %rax	movl	\$0, %eax
addq	%rdx, %rax	jmp	.L3
jmp	*%rax	.L2:	
		cmpq	\$12, -8(%rbp)
		ja	.L4
		movq	-8(%rbp), %rax
		leaq	0(,%rax,4), %rdx
		leaq	.L6(%rip), %rax
		movl	(%rdx,%rax), %eax
		cltq	
		leaq	.L6(%rip), %rdx
		addq	%rdx, %rax
		jmp	*%rax

Finally, the **movl** and **cltq** instructions, along with the first of the earlier **leaq** instructions, do what the **movslq** instruction did in the O1 version. The **movl** instruction copies the offset-table entry into (32-bit) %eax. The **cltq** is a rather obscure instruction that sign extends the value in %eax so that it fills the entire (64-bit) %rax. Then the address of the offset table is computed (again) via the **leaq** instruction.

The final two instructions do what the final two instructions do for the O1 code: they add the offset obtained from the table to the address of the table, then jump to the resulting address.

0x555555555569 <switch eq+4=""></switch>	mov	%rdi,-0x8(%rbp)	
0x5555555555516d <switch eq+8=""></switch>	mov	%rsi,-0x10(%rbp)	
0x5555555555171 <switch eq+12=""></switch>	cmpq	\$0x0,-0x10(%rbp)	
0x5555555555176 <switch eq+17=""></switch>	ja	0x555555555517f <nswi< th=""><th>itch+26></th></nswi<>	itch+26>
0x5555555555178 <switch eq+19=""></switch>	mov	\$0x0,%eax	
0x555555555517d <switch eq+24=""></switch>	jmp	0x5555555551ee <nswi< th=""><th>itch+137></th></nswi<>	itch+137>
0x555555555517f <switch eq+26=""></switch>	cmpq	\$0xc,-0x8(%rbp)	
0x5555555555184 <switch eg+31=""></switch>	ja	0x5555555551e9 <nswi< th=""><th>itch+132></th></nswi<>	itch+132>
0x5555555555186 <switch_eg+33></switch_eg+33>	mov	-0x8(%rbp),%rax	
0x555555555518a <switch_eg+37></switch_eg+37>	lea	0x0(,%rax,4),%rdx	
0x5555555555192 <switch_eg+45></switch_eg+45>	lea	0xe6b(%rip),%rax	# 0x5555555
0x5555555555199 <switch_eg+52></switch_eg+52>	mov	(%rdx,%rax,1),%eax	
0x555555555519c <switch_eg+55></switch_eg+55>	cltq		
0x555555555519e <switch_eg+57></switch_eg+57>	lea	0xe5f(%rip),%rdx	# 0x5555555
0x55555555551a5 <switch_eg+64></switch_eg+64>	add	%rdx,%rax	
>0x55555555551a8 <switch_eg+67></switch_eg+67>	jmp	*%rax	
0x555555556014: -3632 -36		3653 -3674 3632 -3674 3674 -3632	
0x555555556034: -3674 173	4439765		

So, now that we know how switch statements are implemented, how might we "reverse engineer" object code to figure out the switch statement it implements?

Here we're running gdb on a program that contains a call to **switch_eg**. We gave the command "layout asm" so that we can see the assembly listing at the top of the slide. We set a breakpoint at *switch_eg*.

Assuming no knowledge of the original source code, we look at the code for **switch_eg** and see an indirect jump instruction at switch_eg+67, which is a definite indication that the C code contained a switch statement. We can see that %rdx contains the address of the offset table, and that %rax will be set to the entry in the table at the index given in %rdi. The contents of %rdx are added to %rax, thus causing %rax to point to the instruction the indirect jump will go to.

So, with all this in mind, after the breakpoint was reached, we issued the **stepi** (si) command 15 times so that we could see the values of all registers just before the indirect jmp. We then used the $\mathbf{x/14dw}$ gdb command to print 14 entries of a jump offset table starting at the address contained in %rdx. We had to guess how many entries there are – 14 seems reasonable in that it seems unlikely that a switch statement has more than 14 cases, though it might. We know that the table comes after the executable code, so the entries are negative. We see seven entries with values reasonably close to one another, while the remaining entry is very different, so we conclude that the jump table contains13 entries.

0x55555555551a5 <switch eq+64=""></switch>	add	%rdx,%rax	
0x555555555551a8 <switch eq+67=""></switch>	jmp	*%rax	
0x55555555551aa <switch eg+69=""></switch>	cmpq	\$0x1f,-0x10(%rbp)	
0x5555555551af <switch_eg+74></switch_eg+74>	jle	0x5555555551b8 <nswitch+83></nswitch+83>	
0x5555555551b1 <switch_eg+76></switch_eg+76>	mov	\$0x0,%eax	
0x5555555551b6 <switch_eg+81></switch_eg+81>	jmp	0x55555555551ee <nswitch+137></nswitch+137>	
0x5555555551b8 <switch_eg+83></switch_eg+83>	mov	\$0x1,%eax	
0x5555555551bd <switch_eg+88></switch_eg+88>	jmp	0x55555555551ee <nswitch+137></nswitch+137>	
0x5555555551bf <switch_eg+90></switch_eg+90>	cmpq		
0x5555555551c4 <switch_eg+95></switch_eg+95>	jle	0x55555555551cd <nswitch+104></nswitch+104>	
(gdb) x/14dw \$rdx			
		3653 -3674	
0x555555556014: -3632 -	- 3674 -3	3632 -3674	
	-3632 -3	3674 -3632	
0x555555556024: -3674 -	JUJZ -	0002	

The code for some case of the switch should come immediately after the **jmp** (what else would go there?!). So the smallest (most negative) offset in the jump offset table must be the offset for this first code segment. Thus offset -3674 corresponds to switch_eg+69 in the assembly listing. It's at indices 1, 3, 5, 7, 8, 10, and 12 of the table, so it's this code that's executed when the first argument of switch_eg is 1, 3, 5, 7, 8, 10, or 12.

Knowing this, we can figure out the rest.

Quiz 1

What C code would you compile to get the following assembler code?

- ·	50, %rax				
addq \$ cmpq \$	srax, a(,%rax,8) 51, %rax 510, %rax 512	<pre>long a[10]; void func() { long i=0; switch (i) { case 0:</pre>			
<pre>long a[10]; void func() { long i=0; while (i<10) a[i]= i++; }</pre>	<pre>long a[10]; void func() { long i; for (i=0; i<10; i++) a[i]= 1; }</pre>	<pre>a[i] = 0; break; default: a[i] = 10 } }</pre>			
<u> </u>	b	C			
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